

Sub Dcmt
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a capacitor comprising an electrode having a layer comprising platinum-rhodium material and a non-oxide layer comprising platinum material on top of the platinum-rhodium layer, wherein the electrode has a lateral surface aligned with the source/drain region; and

a conductive plug providing electrical contact between the source/drain region and the lateral surface of the electrode.

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60. (amended) The memory cell of claim 55, wherein the titanium layer has a thickness within the range of about 60 to about 100 Angstroms.

Please add new claims 124-125.

124. (new) A memory cell, comprising:

a substrate;

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a transistor including a gate on said substrate and a source/drain region in said substrate disposed adjacent to said gate;

a capacitor comprising an electrode having a titanium layer beneath a platinum-rhodium layer and a platinum layer on top of the platinum-rhodium layer, wherein a titanium nitride layer is provided beneath the titanium layer; and

a conductive plug providing electrical contact between the source/drain region and the lateral surface of the electrode.

125. (new) A memory cell, comprising:

a substrate;

a transistor including a gate on said substrate and a source/drain region in said substrate disposed adjacent to said gate;

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a capacitor comprising an electrode having a titanium nitride layer provided beneath a platinum-rhodium layer and a platinum layer on top of the platinum-rhodium layer, wherein the titanium nitride layer is from about 100 to about 150 Angstroms thick; and

a conductive plug providing electrical contact between the source/drain region and the lateral surface of the electrode.
